AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [38] on pages 10-11 with the following amended paragraph:

[38] Figure 2 is drawing illustrating the construction of a predistortion digital linearizer in accordance with a first embodiment of the present invention. As shown in Figure 2, a predistortion digital linearizer (PDL) preferably includes a predistorter 10[[,]] to distort a digital input signal so that the digital input signal has a distortion characteristic opposite to a nonlinear distortion characteristic of a high power amplifier (HPA) 30. The PDL further includes an up-converter 20[[,]] to up-convert the output signal of the predistorter 10 into a radio frequency (RF) signal, a HPA 30 for power-amplifying the RF signal outputted from the up-converter 20. Next, a feedback unit 40 is provided for feeding back the signal outputted from the HPA 30 and down-converting it. An adaptation processing unit 50 is also provided for controlling predistorting of the digital input signal by using a baseband signal outputted from the feedback unit 40 and the digital input signal which has been delayed for a predetermined time.

Please replace paragraph [43] on page 12 with the following amended paragraph:

[43] Figure 3 shows additional detail of the predistorter 10. As shown in Figure 3, the predistorter 10 preferably includes a power measuring unit 110 to measure the magnitude of an input signal, and a work function generator 120 to generate a predistortion work function for determining a distortion size of the input signal depending on the magnitude of the input signal. The predistorter 10 further ~~icnludes~~ includes a complex coupler 130 for complex-coupling the

predistortion work function generated from the work function generator 120 and the input signal to predistort the input signal.

Please replace paragraph [77] on page 20 with the following amended paragraph:

[77] Referring to Figure 6, the gain control circuit 200 preferably includes a first multiplier 210 that multiplies the first phase digital input signal (signal I) with the gain control signal to control the level of the first phase digital input signal, and a first rounding unit 220 that takes a predetermined number of bits from the digital output signal of the first multiplier 210, and adjusts an input and output digit. The gain control circuit also includes a second multiplier [[220]] 230 that multiplies the second phase digital input signal (signal Q) with the gain control signal to control the level of the second phase digital input signal, and a second rounding unit 240 that takes a predetermined number of bits from the digital output signal of the second multiplier [[220]] 230, and adjusts an input and output digit.